1. A method of forming a bonding pad that is immune to IMD cracking, comprising:

providing a partially processed semiconductor wafer having all metal levels completed;

forming a blanket dielectric layer over the uppermost metal level;

patterning and etching said dielectric layer to form horizontal and vertical arrays of trenches passing through said dielectric layer and separating said dielectric layer into cells;

filling said trenches with a conducting material;

performing CMP;

depositing bonding metal patterns;

bonding wires onto said bonding metal patterns;

forming a passivation layer.

2. The method of Claim 1 wherein said dielectric layer is composed of materials from the set: silicon oxide, silicon nitride, silicon oxynitride.

3. The method of Claim 1 wherein said dielectric layer is a composite of dielectric layers.

4. The method of Claim 1 wherein said dielectric layer is a composed of two layers, an oxide layer formed using HDP and an oxide layer formed using DCTEOS.

5. The method of Claim 1 wherein said dielectric layer is a composed of two layers, an oxide layer formed using SACVD and an oxide layer formed using HSTEOS.

6. The method of Claim 1 wherein the filling of said trenches with a conducting material is accomplished using a plug process.

7. The method of Claim 1 wherein the filling of said trenches with a conducting material is accomplished using a W plug process.

Sub A2

8. The method of Claim 1 wherein the filling of said trenches with a conducting material is accomplished using a plug process from the set: AL plug, Cu plug, silicide plug.

9. The method of claim 1 wherein the width of said trenches is between 0.1 and 0.5 micrometers.

10. The method of claim 1 wherein the separation between neighboring horizontal trenches and neighboring vertical trenches is between 0.2 and 20 micrometers.

Sub A3

11. A method of forming a bonding pad that is immune to IMD cracking, comprising:

providing a partially processed semiconductor wafer having all metal levels completed;

forming a blanket dielectric layer over the uppermost metal level;

patterning and etching said dielectric layer to form horizontal and vertical arrays of trenches passing through said dielectric layer according to the nonintersecting layout;

filling said trenches with a conducting material;

performing CMP;

depositing bonding metal patterns;

bonding wires onto said bonding metal patterns;

forming a passivation layer.

12. The method of Claim 11 wherein said dielectric layer is composed of materials from the set: silicon oxide, silicon nitride, silicon oxynitride.

13. The method of Claim 11 wherein said dielectric layer is a composite of dielectric layers.

14. The method of Claim 11 wherein said dielectric layer is a composed of two layers, an oxide layer formed using HDP and an oxide layer formed using DCTEOS.

15. The method of Claim 11 wherein said dielectric layer is a composed of two layers, an oxide layer formed using SACVD and an oxide layer formed using HSTEOS.

16. The method of Claim 11 wherein the filling of said trenches with a conducting material is accomplished using a plug process.

17. The method of Claim 11 wherein the filling of said trenches with a conducting material is accomplished using a W plug process.

18. The method of Claim 11 wherein the filling of said trenches with a conducting material is accomplished using a plug process from the set: AL plug, Cu plug, silicide plug.

19. The method of claim 11 wherein the width of said trenches is between 0.1 and 0.5 micrometers.

20. The method of claim 11 wherein the separation between neighboring horizontal trenches and neighboring vertical trenches is between 0.1 and 10 micrometers, and the ratio between the spacing of perpendicular trenches to the spacing of

parallel trenches is less then about 1/5, and the spacing of perpendicular trenches is greater then about 0.1 micrometers

21. A method of forming a bonding pad that is immune to IMD cracking, comprising:

providing a partially processed semiconductor wafer having all metal levels completed;

forming a blanket dielectric layer over the uppermost metal level;

patterning and etching said dielectric layer to form horizontal and vertical arrays of trenches passing through said dielectric layer according to the brick laying layout or the modified brick laying layout;

filling said trenches with a conducting material;

performing CMP;

depositing bonding metal patterns;

bonding wires onto said bonding metal patterns;

forming a passivation layer.

22. The method of Claim 21 wherein said dielectric layer is composed of materials from the set: silicon oxide, silicon nitride, silicon oxynitride.

23. The method of Claim 21 wherein said dielectric layer is a composite of dielectric layers.

24. The method of Claim 21 wherein said dielectric layer is a composed of two layers, an oxide layer formed using HDP and an oxide layer formed using DCTEOS.

25. The method of Claim 21 wherein said dielectric layer is a composed of two layers, an oxide layer formed using SACVD and an oxide layer formed using HSTEOS.

26. The method of Claim 21 wherein the filling of said trenches with a conducting material is accomplished using a plug process.

27. The method of Claim 21 wherein the filling of said trenches with a conducting material is accomplished using a W plug process.

28. The method of Claim 21 wherein the filling of said trenches with a conducting material is accomplished using a plug process from the set: AL plug, Cu plug, silicide plug.

29. The method of claim 21 wherein the width of said trenches is between 0.1 and 0.5 micrometers.

30. The method of claim 21 wherein the separation between neighboring horizontal trenches is between 0.1 and 10 micrometers and neighboring vertical trenches is between 0.1 and 10 micrometers.

31. The method of Claim 21 wherein the overlap area in said modified bricklaying layout is between 0.1 and 1 of the overlap area of said bricklaying layout.